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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,951	07/25/2006	Takeshi Ishigaki	SUZU1720	3389

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EXAMINER	
ROJAS, DANIEL E	
ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
10/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,951	ISHIGAKI, TAKESHI	
	Examiner	Art Unit	
	DANIEL ROJAS	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-8* is/are allowed.

6)☒ Claim(s) *9* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 10, filed 7/3/3008, with respect to the drawing objections and rejection under 35 U.S.C. § 112 have been fully considered and are persuasive. The drawing objection and rejection of under 35 U.S.C. § 112 of Figure 1-20 and claims 6, 9, and 10 respectively have been withdrawn.

2. Applicant's arguments regarding the rejection under 35 U.S.C. § 102 filed 7/3/2008 have been fully considered but they are not persuasive. Applicant argues that it appears as though no counter signal is supplied to reset generation circuitry 26. The details of the reset signal generation circuitry are shown in Figure 4. 26 receives the MASTER DIVIDER SIGNAL which is the output of counter 25, as shown in Figure 3. 26 is defined as the second circuit in the second circuit area in the previous office action. The D flip flop within 34 is defined as the first circuit in the previous office action. Figure 2 shows that 30 provides a signal to the first circuit (34) in the first area (14) which is determined in part by the output of 26.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Arnould et al (US Patent No. 6,118,314), hereinafter referred to as Arnould.

5. For claim 9, Arnould teaches a circuit (Figure 2) comprising: a semiconductor substrate having a first area (14) and a second area (12); a plurality of counters (as explained below) one of which is provided in the first area and the second area (within 24 and 34, as explained below) and which cyclically count a same value at a same timing and output a counter signal as a result of counting (as explained below); a first circuit (D flip flop within 34, as explained below) provided in the first area, supplied with a first counter signal (identically to what is shown in Figure 3, as explained below) from the one of the counters in the first area and outputting a first signal when the first counter signal has a first value (inherent based upon the structure); and a second circuit (26) provided in the second area, supplied with a second counter signal from the one of the counters in the second area (as shown in Figures 2, 3, and 4) and supplying the first circuit with a second signal (17, via 30) containing information on a value of the second counter signal obtained upon reception of the first signal (inherent based upon the structure). Arnould's specification states that "slave divider 34 can comprise the configuration of master divider 24 shown in Fig. 3" (column 6, lines 37-39). Therefore, Figure 3 shows the details of both the master divider and slave divider, wherein the signals master local clock, master internal clock, and master divider signal are replaced with slave local clock, slave internal clock, and slave divider signal for 34, respectively. Arnould further teaches that "master divider 24 and slave divider 34 are individually configured to divide the master local clock and slave local clock by three" (column 4, lines 53-55) and that the "master local clock signal and slave local clock signal individual have a frequency which is four times the frequency of the reference clock

signal" (column 4, lines 33-36). Therefore, the counter in the first area and the counter in the second area are receiving identical clock signals from their respective phase lock loop circuits. Thus, the two said counters cyclically count the same value at a same timing. Arnould teaches that "following assertion of reset detection signal 74 (output of 48, Figure 5), slave divider 34 is set to position one and begins counting position one, position two, position zero, position one, etc." (column 8, lines 31-34). Therefore, the second circuit 26 supplied with a counter signal (as shown in Figure 2) supplies the first circuit (26 of the slave divider, Figure 3) with a second signal (reset slave, Figure 5) which contains information on a value of a counter signal (i.e. reset signal) obtained upon reception of the first signal (inherent based on structure).

Allowable Subject Matter

6. Claims 6-8 are allowed.

7. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/D. R./
Examiner, Art Unit 2816
10/8/2008